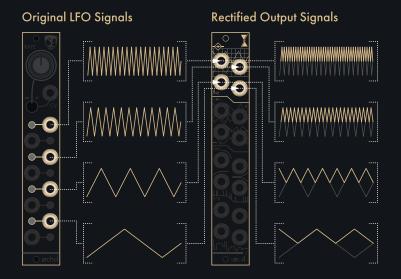




#### Full Wave Rectifiers ———

All negative portions of the LFOs are inverted resulting in unipolar positive signals at the expander outputs (0-5 volts).



### Analogue Diode Logic Pairs ——

The max/min outputs produce a bi-polar -5 to +5 volt signal. The top two channels (max) output whichever is currently the highest voltage of the original LFO input pair. The bottom two channels (min) output whichever is currently the lowest voltage of the original LFO input pair.

## **Original LFO Signals Diode Logic Output Signals**

## Cascading Triggers ——



Produces ~8ms triggers at the start of the rising edge of the LFO signals. Clockwise cascading normalisation through the outputs results in a layering of trigger signals if the previous output is left unpatched.

# **Original LFO Signals Trigger Signals**

#### R-2R 4-bit Ladder DACs

There are two factors at play that impact the DAC outputs. Firstly, the rate of the LFOs set the rate of the random signals. Secondly, the ordering of Most Significant Bit (MSB) to Least Significant Bit (LSB) effects the size and rate of voltage change. The following clusters from the øchd will produce four different flavours of random voltage (slow noise) from the øchd expander.

